

19. The structure according to claim 17 wherein said soft metal conductor is selected from the group consisting of Cu, Al, Ag and alloys thereof.

20. The structure of claim 17 wherein said plated multigrained soft metal conductor is an electroplated multigrained soft metal conductor.

21. The structure of claim 17 wherein said plated multigrained soft metal conductor is an electrolessly plated multigrained soft metal conductor.

22. A semiconductor structure comprising a conductive metal line, said metal line interconnecting devices in a semiconductor chip, said metal line having low electrical resistance and being comprised of a plated soft metal, said plated soft metal having an upper surface, said upper surface being a polished surface, said metal line comprised of grains, said grains sufficiently large so as to prevent substantial scratching of said upper surface during polishing.

23. The structure according to claim 22 wherein said soft metal is selected from the group consisting of Cu, Al, Ag and alloys thereof.

24. The structure according to claim 22 wherein said soft metal is selected from the group consisting of Cu and alloys thereof.

25. The structure according to claim 22 wherein said plated soft metal is an electroplated soft metal.

26. The structure according to claim 22 wherein said plated soft metal is an electrolessly plated soft metal.

27. The structure according to claim 22 wherein said conductive metal line is formed using a damascene process.

28. The structure according to claim 22 wherein said conductive metal line is formed using a dual damascene process.

29. An interconnecting structure of a semiconductor chip, the chip including a layer of semiconducting material having devices therein, the interconnecting structure comprising:

a first electrically conductive layer electrically contacting at least one device;  
a second electrically conductive layer overlying and contacting said first  
electrically conductive layer, said second electrically conductive layer being formed in an  
insulator overlying said first electrically conductive layer, said second conductive layer  
being a plated soft metal having an upper surface, said upper surface being a polished  
surface, said second electrically conductive layer comprised of grains, said grains  
sufficiently large so as to prevent substantial scratching of said upper surface during  
polishing.

30. The structure according to claim 29 wherein at least a portion of said individual  
grains comprising said second conductive layer have a size of at least about 200 nm.

31. The structure according to claim 29 wherein said plated soft metal is selected from  
the group consisting of Cu, Al, Ag and alloys thereof.

32. The structure according to claim 29 wherein said plated soft metal is selected from  
the group consisting of Cu and alloys thereof.

33. A semiconductor structure, comprising:

a semiconductor chip having devices therein; and  
a plated soft metal layer interconnecting said devices, said soft metal selected  
from the group consisting of Cu and alloys thereof, said soft metal layer having a  
polished substantially scratch free surface.

34. The semiconductor structure according to claim 33 wherein said soft metal layer is a  
damascene layer.